EXAMINER'S AMENDMENT

1. Claims 2-7, 9-12, 14-22, 24-35, and 38-42 are pending the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John A Garrity on March 20, 2009.

The application has been amended as follows wherein the following versions of claims 6, 10, 11, 15-17, 19, 20, 25-30, 32, 34, 38, 39, 40, and 41 replace all prior versions in their entirety and claims 7 and 21 are cancelled:

6. The power synthesizer of claim 10, wherein for each of the n stages, the discrete amplitude amplifier of the n^{th} stage has an input that is directly coupled to an output of the modulator of the n^{th} stage.

7. (CANCELLED) ~~The power synthesizer of claim 10 further comprising the discrete amplitude generator having parallel outputs coupled to inputs of the n stages~~

10. A power synthesizer comprising a plurality of n stages in parallel with one another, wherein n is an integer at least equal to two, each of the n stages comprising:

a modulator and a discrete amplitude amplifier in series with one another,

each n^{th} discrete amplitude amplifier configured to apply a gain that is unique as compared to all other of the discrete amplitude amplifiers; and

~~an~~ a common actuator configured to simultaneously switch the n modulators, wherein

each of the modulators is coupled to ~~a~~ the common actuator, and

each n[th] discrete amplitude amplifier is configured to output a signal amplitude $a_0 / 2^{n-1}$, where a_0 is a maximum signal amplitude output by any of said n discrete amplitude amplifiers;

the power synthesizer further ~~comprising~~ comprises a discrete amplitude generator configured to convert a real valued input to a first and second parallel binary outputs that are each coupled to an input of ~~the~~ a respective one of the n modulators ~~n[th] modulator~~.

11. A power synthesizer comprising a plurality of n stages in parallel with one another, wherein n is an integer at least equal to two, each of the n stages comprising:

a modulator and a discrete amplitude amplifier in series with one another,

each n[th] discrete amplitude amplifier configured to apply a gain that is unique as compared to all other of the discrete amplitude amplifiers; and

an actuator configured to simultaneously switch the n modulators, wherein, in one stage, the discrete amplitude amplifier comprises x FETs each having a drain and a gate, and in another stage, the discrete amplitude amplifier comprises x/2 FETs each having a drain and a gate, wherein x is an even integer greater than two, wherein the drains of the x FETs of the discrete amplitude amplifier of the one stage ~~have~~ are coupled in parallel ~~one of gates and drains~~, and wherein the gates of the x/2 FETs of the discrete amplifier of the another stage ~~have~~ are coupled in parallel ~~one of gates and drains~~.

15. The apparatus of claim 38, wherein each of the ~~at least two~~ n discrete amplifier stages comprises a discrete amplitude amplifier and a modulator in series with one another.

16. The apparatus of claim 15, further comprising an inverse fast fourier transform IFFT block disposed between the serial to parallel converter and the parallel to serial converter, the ~~power synthesizer block further comprising a~~ discrete amplitude generator configured to convert a real valued ~~input~~ output from the IFFT block to parallel binary outputs~~, each parallel binary output coupled to an input of a modulator~~.

17. The apparatus of claim 38, wherein the power synthesizer block further comprises at least one power combiner configured to couple an output of each of the ~~at least two~~ n discrete amplifier stages with at least one transmit antenna.

19. The apparatus of claim 38, wherein each of the discrete amplitude amplifiers comprises a constant envelope amplifier.

20. The apparatus of claim 17, ~~wherein the at least one transmit antenna comprises a first and a second transmit antenna,~~ wherein ~~an~~ each output of ~~one of~~ the ~~at least two~~ n discrete amplifier stages is coupled to an input of ~~the first transmit~~ an antenna ~~and an output of another of the at least two discrete amplifier stages is coupled to an input of the second transmit antenna~~.

21.(CANCELLED) ~~The apparatus of claim 20, wherein the at least two transmit antennas comprise n transmit antennas and the at least two discrete amplifier stages comprise n discrete amplifier stages, wherein each n^{th} transmit antenna is coupled to an output of an n^{th} discrete amplifier stage~~.

25. The method of claim 40, wherein ~~controlling a~~ phase ~~of the~~ modulating an input bit comprises spectrally shaping the input bit with a continuous phase modulator.

26. The method of claim 25 wherein the continuous phase modulator comprises a pulse amplitude modulator.

27. The method of claim 25 wherein the continuous phase modulator approximately performs Gaussian minimum shift keying.

28. The method of claim 25 ~~further comprising, previous to providing a separate bit of a bit stream, converting~~ wherein the real valued input is an amplitude modulated signal ~~to the bit stream~~.

29. The method of claim 40, wherein combining the phase modulated and amplified ~~phase controlled~~ bits in a circuit manner comprises combining all of the n phase modulated and amplified ~~and phase controlled~~ bits with at least one power combiner prior to transmission.

30. The power synthesizer of claim 10 wherein each ~~of the~~ ~~n~~th discrete amplitude ~~amplifiers apply~~ amplifier applies a gain that differs from that applied by another nearest-gain ~~nearest-power~~ discrete amplitude amplifier by a fixed amount.

32. The apparatus of claim 38, wherein each discrete amplitude amplifier is configured to apply a gain that differs by a fixed amount from that applied by its nearest-gain neighbor discrete amplitude amplifier.

34. The method of claim 40, wherein amplifying each phase modulated bit at ~~a power of the input bit at~~ a power that is unique respecting all other n parallel inputs comprises, for each of the n parallel inputs, amplifying with a power that differs by a fixed amount from a next nearest power amplification.

38. An apparatus comprising, in series: an encoder, a serial to parallel converter, and a parallel to serial converter configured to output a digital signal at baseband, the apparatus further comprising:

a power synthesizer block comprising n ~~at least two~~ discrete amplifier stages in parallel, ~~each stage disposed between the parallel to serial converter, and~~ wherein each discrete amplifier stage comprises a discrete amplitude amplifier configured to apply a gain that differs from that applied by each other discrete amplitude amplifier of each other discrete amplifier stage, wherein n is an integer of at least 2 ~~each of the stages comprises an n~~th ~~stage~~ and each nth discrete amplifier stage comprises a modulator,

each of the modulators is connected to a common actuator; and

each of the nth discrete amplitude amplifiers is configured to output a signal amplitude $a_0/2^{n-1}$, where a_0 is a maximum signal amplitude output by any of said n discrete amplitude amplifiers, and where

the power synthesizer block further comprises a discrete amplitude generator configured to convert a real valued input to ~~n~~ a first and second parallel binary outputs that are each coupled to an input of ~~the~~ a respective one of the n modulators ~~n^th^ modulator~~.

39. The apparatus of claim 38 wherein, in one discrete amplifier stage, the discrete amplitude amplifier comprises x FETs each having a drain and a gate, and in another discrete amplifier stage, the discrete amplitude amplifier comprises x/2 FETs each having a drain and a gate, wherein x is an even integer greater than two, wherein the drains of the x FETs of the discrete amplitude amplifier of the one discrete amplifier stage ~~have~~ are coupled in parallel ~~one of gates and drains~~, and wherein the gates of the x/2 FETs of the discrete amplifier of the another discrete amplifier stage ~~have~~ are coupled in parallel ~~one of gates and drains~~.

40. A method comprising:

converting a real valued input to a bit stream;

providing a separate bit of ~~a~~ the bit stream on each of n parallel inputs wherein each bit of the bit stream ~~representing~~ represents a different significance;

for each of the n parallel inputs, ~~controlling a~~ performing phase modulation ~~of~~ according to the input bit and amplifying the phase modulated bit by an n^th^ discrete amplitude amplifier ~~a power of the input bit at~~ having a power that is unique respecting all other n parallel inputs; and

combining all n phase modulated ~~controlled~~ and amplified bits in one of a spatial transmission manner and a circuit manner, wherein the phase modulation ~~controlling a phase of each of the n parallel inputs~~ is controlled by a common actuator; and each n^th^ discrete amplitude amplifier is adapted to output a signal amplitude $a_0 / 2^{n-1}$, where a_0 is a maximum signal amplitude output by any of said discrete amplitude amplifiers~~; and converting a real valued input to the n parallel input bit streams~~.

41. A method comprising:

providing a separate bit of a bit stream on each of n parallel inputs wherein each bit of the bit stream ~~representing~~ represents a different significance;

for each of the n parallel inputs, ~~controlling a~~ performing phase modulation ~~of~~ according to the input bit and amplifying the phase modulated bit by an n^{th} discrete amplitude amplifier ~~a power of the input bit at~~ having a power that is unique respecting all other n parallel inputs; and

combining all n phase modulated ~~controlled~~ and amplified bits in one of a spatial transmission manner and a circuit manner, wherein~~, in~~ one of the n discrete amplitude amplifiers comprises x FETs each having a drain and a gate, and an other of the n discrete amplitude amplifiers comprises x/2 FETs each having a drain and a gate, wherein x is an even integer greater than two, wherein the drains of the x FETs of the discrete amplitude amplifier of the one stage ~~have~~ are coupled in parallel ~~one of gates and drains~~, and wherein the gates of the x/2 FETs of the discrete amplifier of the another stage ~~have~~ are coupled in parallel ~~one of gates and drains~~.

Independent claims 10, 11, 38, 40, and 41 are renumbered respectively as claims 1, 11, 12, 24, and 34. The dependent claims (including their dependencies) are renumbered accordingly.

Allowable Subject Matter

3. Claims 2-6, 9-12, 14-20, 22, 24-35, and 38-42 renumbered as claims 1-34 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JASON M. PERILLA whose telephone number is (571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Jason M Perilla/
Primary Examiner, Art Unit 2611
March 23, 2009

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